4- P-N Junction

We begin our study of semiconductor devices with the junction for three reasons.

(1) The device finds application in many electronic systems, e.g., in adapters that charge the batteries of cell phones.

(2) The *pn* junction is among the simplest semiconductor devices, thus providing a good entry point into the study of the operation of such complex structures as transistors.

(3) The *pn* junction also serves as part of transistors.

Figure 4.1 shows the joining of two semiconductors (p and n-types) together to form the meaning of a p-n junction which is so called a Diode.

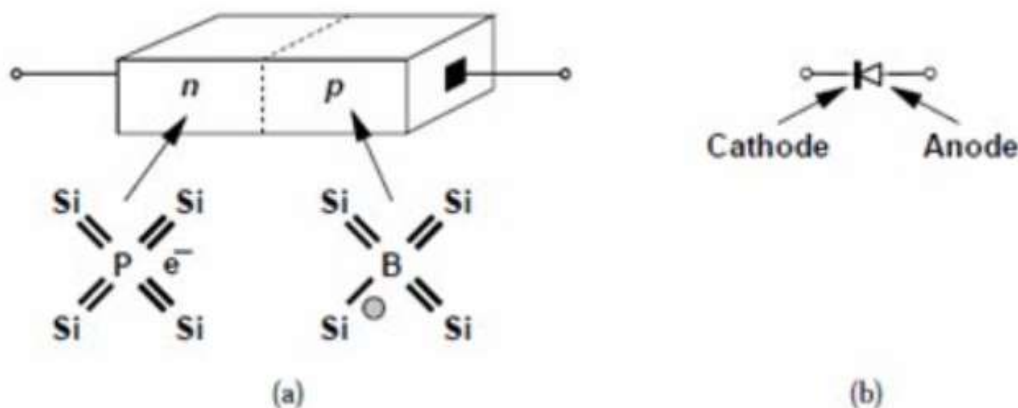


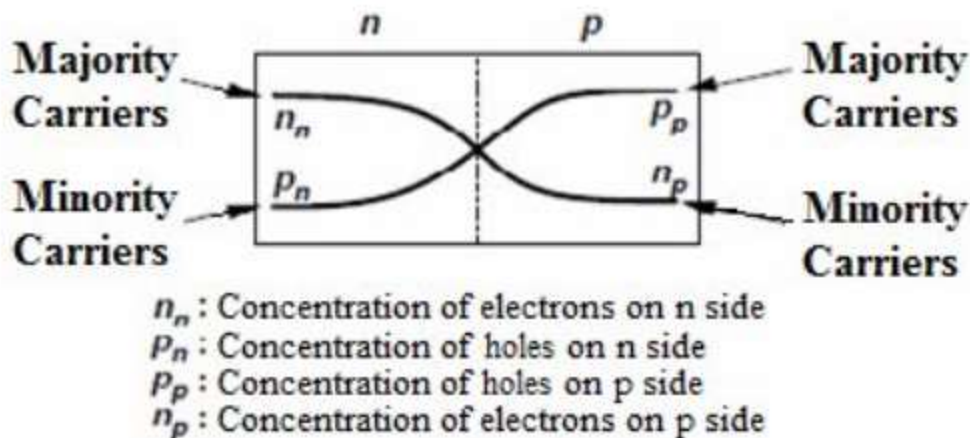
Figure 4.1 Diode p-n junction

4.1 PN Junction in Equilibrium

Let us first study the *pn* junction with no external connections, i.e., the terminals are open and no voltage is applied across the device. We say the junction is in "***equilibrium***". While of no practical value, this condition provides insights that prove useful in understanding the operation under *no equilibrium* as well.

Example 4.1:

A *pn* junction employs the following doping levels: $N_A= 10^{16}$ cm^{-3} and $N_D=5$ x 10^{15} cm^{-3}. Determine the hole and electron concentration on both sides of the pn junction.



Solution:

For the P side note that $p_p=N_A$ and therefore:

$$n_p = \frac{n_i^2}{N_A} = \frac{(1x10^{10})^2}{10^{16}} = 10^4\ cm^{-3}$$

Same manner at the n type region, n_n=N_D and the minority concentration of holes is ;

$$p_n = \frac{n_i^2}{N_D} = \frac{(1x10^{10})^2}{5x10^{15}} = 2x\ 10^4\ cm^{-3}$$

4.2 Built-in Potential:

The existence of an electric field within the depletion region suggests that the junction may exhibit a “built-in potential”. Figure 4.2 shows carrier profiles in a p-n junction with majority and minority concentrations at each side.

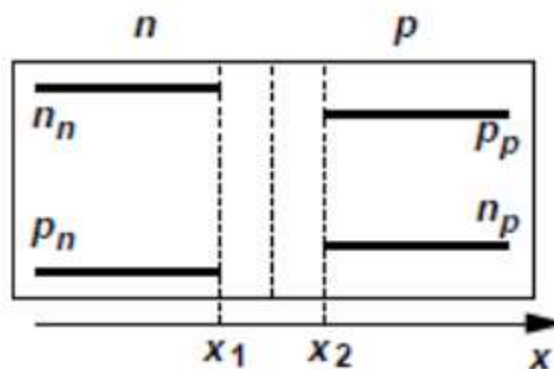


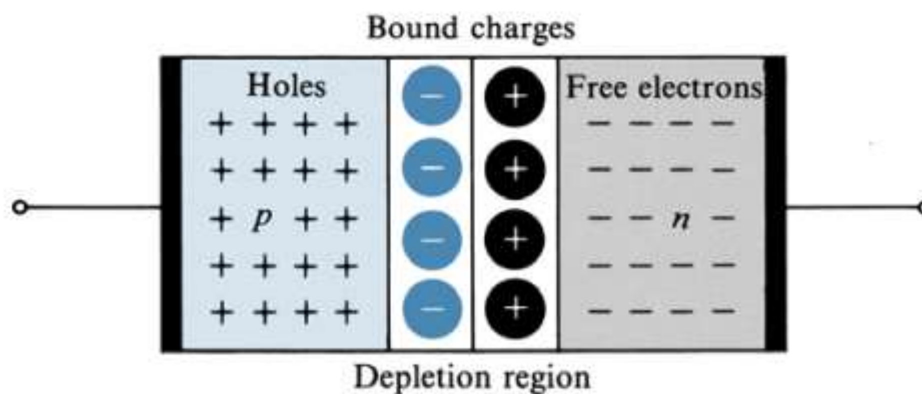
Figure 4.2 carrier profiles in a p-n junction

Expressing the built-in potential in terms of junction parameters, this equation plays a central role in many semiconductor devices. Therefore the built-in voltage (the voltage across the deplation region) V_o is given by;

$$V_o = \frac{kT}{q}\,\frac{\ln(N_A N_D)}{n_i^2}$$

Note that ; $V_T = \frac{kT}{q} = 26\,mV$ at room temperature (T=300K).

Typically, at room temp, V_o is 0.6~0.8V.



Example 4.2:

A silicon *pn* junction employs N_A=2 x 10^{16} cm^{-3} and N_D=4 x 10^{16} cm^{-3}. Determine the Built in potential voltage at room temperature.

Solution:

Applying the direct equation for the Built-in voltage of a pn junction as following;

$$V_o = 26\, x\, 10^{-3}\ \frac{\ln(2x10^{16}x\ 4\ x\ 10^{16})}{(10^{10})^2} = 0.768\, V = 768\, mV$$

4.3 Width of the Depletion Region (W_{dep})

The depletion region exists on both sides of the junction. The width in each side is a function of the respective doping levels. The width of the depletion region can be found as a function of doping and the built-in voltage as follows;

$$W_{dep} = \sqrt{\frac{2\epsilon_s}{q}(\frac{1}{N_A} + \frac{1}{N_D})V_o}$$

where $\in_s$ is the electrical permittivity of silicon = $11.7\in_o$ F/m

Example 4.3 (H.W):

A silicon *pn* junction employs $N_A=10^{16}$ cm^{-3} and $N_D=5 \times 10^{16}$ cm^{-3}. Determine the Built in potential voltage at room temperature and the depletion region width.

4.4 *PN* Junction under Reverse Bias

For the case of reverse bias, we note that in Figure 4.3, as V_R increases, more positive charge appears on the (n) side and more negative charge on the (p) side.

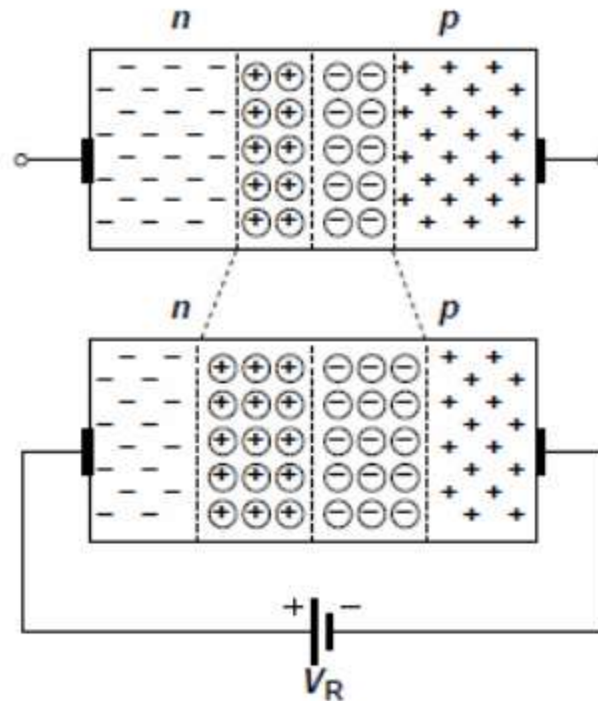


Figure 4.3 pn junction under reverse bias

Thus, the device operates as a capacitor as shown in Figure 4.4. In essence, we can view the conductive n and p sections as the two plates of the capacitor. We also assume the charge in the depletion region equivalently resides on each plate.

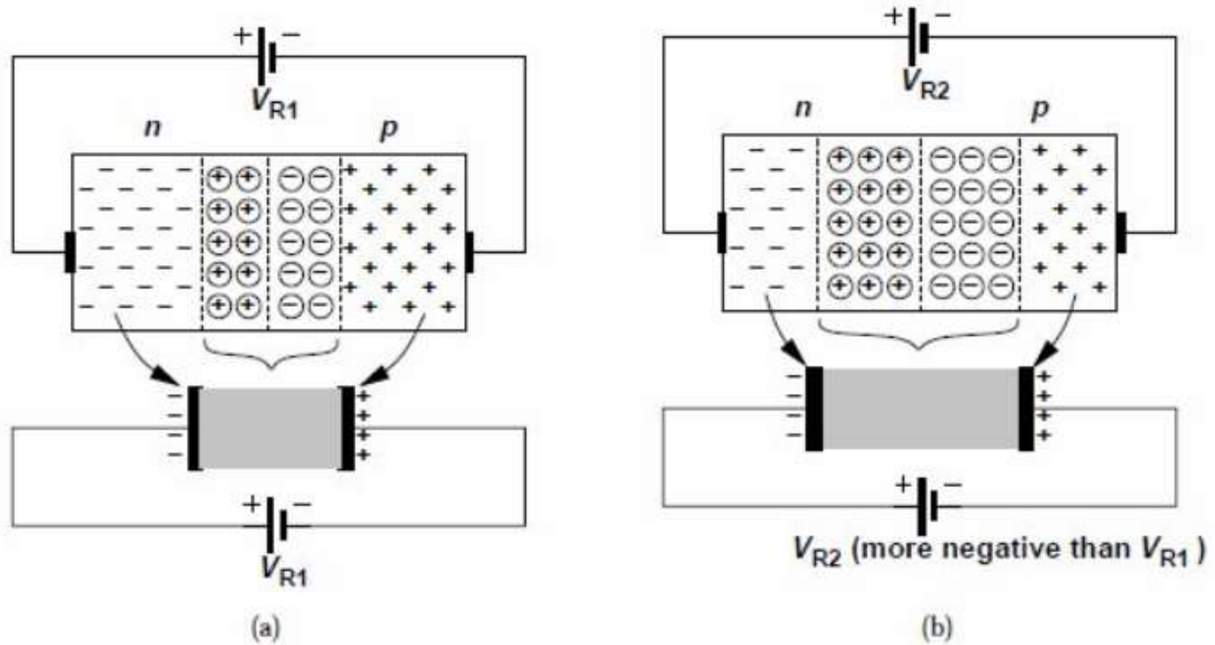


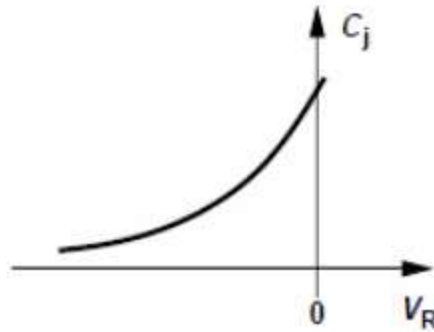
Figure 4.4 Reduction of junction capacitance with reverse bias

Since any two parallel plates can form a capacitor, for increasing values of V_R revealing that the capacitance of the structure *decreases* as the two plates move away from each other. The junction therefore displays a voltage-dependent capacitance. It can be proved that the capacitance of the junction per unit area is equal to;

$$C_j = \frac{C_{jo}}{\sqrt{1 - \frac{V_R}{V_o}}}$$

where C_{jo} denotes the capacitance corresponding to zero bias (V_R=0) and V_o is the built in voltage. Defining C_{jo} as ;

$$C_j = \sqrt{\frac{\epsilon_s\, q\, N_A N_D}{2V_o(N_A + N_D)}}$$



Furthermore, as the depletion region grows, the capacitance across the diode changes, therefore;

$$W_{dep} = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_o + V_R)}$$

Example 4.4:

A *pn* junction is doped with N_A=2 x10^{16} cm^{-3} and N_D=9 x 10^{15} cm^{-3}. Determine the capacitance of the device and the depletion region width for (1) V_R=0 and for (2) V_R=1 V.

Solution:

Initially we should obtain the built-in voltage as;

$$V_o = \frac{kT}{q} \frac{\ln(N_A N_D)}{n_i^2} =$$

Thus for V_R=0 V we have;

$$C_j = \sqrt{\frac{\epsilon_s \, q \, N_A N_D}{2V_o(N_A + N_D)}} = 2.65 \, x \, 10^{-8} \, \frac{F}{cm^2}$$

and for V_R=1 V we have;

$$C_j = \frac{C_{jo}}{\sqrt{1 - \frac{V_R}{V_o}}} = 1.72 \, x \; 10^{-8} \, \frac{F}{cm^2}$$